CLAIMS

What is claimed is:

1. A method of making a non-volatile memory comprising:

providing a semiconductor substrate;

forming at least two buried bit lines within the semiconductor substrate, wherein forming the at least two buried bit lines defines boundaries that delineate the at least two buried bit lines from an active region disposed between the buried bit lines;

providing a charge storage layer overlying the semiconductor substrate;

forming a first control gate overlying the charge storage layer; forming an insulating liner overlying the first control gate; and

forming first and second sidewall spacer control gates adjacent to first and second sidewalls of the first control gate, respectively, the first and second sidewall spacer control gates being separated from the first control gate by at least the insulating liner, wherein multi-bit programmable charge storage regions are created within the charge storage layer beneath respective ones of the control gates.

2. The method of claim 1, further comprising:

providing a protective layer overlying the charge storage layer.

3. The method of claim 2, wherein the protective layer includes a nitride layer.

4. The method of claim 1, wherein the charge storage layer includes a charge storage stack.

5. The method of claim 4, wherein the charge storage stack includes at least a bottom insulating layer, charge storage layer, and top insulating layer.

6. The method of claim 5, further wherein the charge storage layer includes at least one selected from the group consisting of a Si_3N_4 layer, a layer consisting of oxynitride, a layer consisting of a plurality of nanocrystals, a layer consisting of a plurality of nanoclusters, and any combinations thereof.

7. The method of claim 4, wherein the charge storage stack includes at least one selected from the group consisting of an ONO stack, an oxide nanocrystal oxide stack, and an oxide nanocluster oxide stack.

8. The method of claim 1, wherein the at least two buried bit lines includes a plurality of buried bit lines.

9. The method of claim 8, wherein the plurality of buried bit lines are formed subsequent to providing of the charge storage layer.

10. The method of claim 1, wherein the first control gate includes at least one conductor selected from the group consisting of polysilicon and metal.

11. The method of claim 1, wherein the first control gate includes polysilicon.

12. The method of claim 1, wherein the insulating liner includes an oxide.

13. The method of claim 1, wherein forming the first control gate includes forming a plurality of first control gates, and

wherein forming the insulating liner includes forming the insulating liner overlying the plurality of first control gates.

14. The method of claim 1, further wherein the multi-bit programmable charge storage regions are positioned a) underlying the first control gate within the charge storage layer and in a region proximate a boundary of a buried bit line and an active region, and b) underlying the first and second sidewall spacer control gates within the charge storage layer and in a region proximate a boundary of a buried bit line and an active region.

15. The method of claim 1, wherein forming the first control gate includes forming a plurality of first control gates, and wherein forming the first and second sidewall spacer control gates includes forming a plurality of first and second sidewall spacer control gates adjacent to sidewalls of individual ones of the plurality of first control gates, wherein individual ones of the first and second sidewall spacer control gates are separated from a respective first control gate by at least the insulating liner.

16. The method of claim 1, wherein forming the first control gate includes forming a plurality of first control gates, and wherein forming the first and second sidewall spacer control gates includes forming the first sidewall spacer control gate on a first sidewall of a desired one of the first control gates, wherein the first sidewall spacer control gate extends between the desired one of the first control gates and an adjacent one of the first control gates, and forming the second sidewall spacer control gate on a second sidewall of the desired one of

the first control gates, wherein the second sidewall spacer control gate further extends between the desired one of the first control gates and an opposite adjacent one of the first control gates.

17. The method of claim 1, wherein forming the first and second sidewall spacer control gates includes depositing a conformal layer of conductive material overlying the first control gate followed by anisotropic etching of the conformal layer.

18. The method of claim 17, wherein the conductive material includes polysilicon.

19. The method of claim 1, further comprising forming a silicide on the first and second sidewall spacer control gates.

20. The method of claim 1, further comprising forming a silicide on the first control gate and on the first and second sidewall spacer control gates.

21. The method of claim 1, wherein the charge storage regions are programmable via a process of hot carrier injection.

22. A non-volatile memory comprising:

a semiconductor substrate;

at least two buried bit lines formed within the semiconductor substrate, wherein the buried bit lines define boundaries that delineate the buried bit lines from an active region disposed between the buried bit lines;

a charge storage layer overlying the semiconductor substrate;

a first control gate overlying the charge storage layer;

an insulating liner overlying the first control gate; and

first and second sidewall spacer control gates formed adjacent to first and second sidewalls of the first control gate, respectively, the first and second sidewall spacer control gates being separated from the first control gate by at least the insulating liner, wherein multi-bit programmable charge storage regions are created within the charge storage layer beneath respective ones of the control gates.

23. The memory of claim 22, further comprising:

a protective layer overlying the charge storage layer and underlying the first control gate.

24. The memory of claim 23, wherein the protective layer includes a nitride layer.

25. The memory of claim 22, wherein the charge storage layer includes a charge storage stack having at least a bottom insulating layer, a charge storage layer, and a top insulating layer.

26. The memory of claim 25, further wherein the charge storage layer of the charge storage stack includes at least one selected from the group consisting of a Si_3N_4 layer, an oxynitride layer, a layer consisting of a plurality of nanocrystals, a layer consisting of a plurality of nanoclusters, and any combinations thereof.

27. The memory of claim 25, wherein the charge storage stack includes at least one selected from the group consisting of an ONO stack, an oxide nanocrystal oxide stack, and an oxide nanocluster oxide stack.

28. The memory of claim 22, wherein the at least two buried bit lines includes a plurality of buried bit lines.

29. The memory of claim 22, wherein the first control gate includes at least one conductor selected from the group consisting of polysilicon and metal.

30. The memory of claim 22, wherein the first control gate includes a plurality of first control gates, and wherein the insulating liner overlies the plurality of first control gates.

31. The memory of claim 22, further wherein the multi-bit programmable charge storage regions are positioned a) underlying the first control gate within the charge storage layer and in a region proximate a boundary of a buried bit line and an active region, and b) underlying the first and second sidewall spacer control gates within the charge storage layer and in a region proximate a boundary of a buried bit line and an active region.

32. The memory of claim 22, wherein the first control gate includes a plurality of first control gates, and wherein the first and second sidewall spacer control gates include a plurality of first and second sidewall spacer control gates adjacent to sidewalls of individual ones of the plurality of first control gates, wherein individual ones of the first and second sidewall spacer control gates are separated from a respective first control gate by at least the insulating liner.

33. The memory of claim 22, wherein the first control gate includes a plurality of first control gates, and wherein the first and second sidewall spacer control gates include the first sidewall spacer control gate formed on a first sidewall of a desired one of the first control gates, wherein the first sidewall spacer control gate extends between the desired one of the first control gates and an adjacent one of the first control gates, and the second sidewall spacer control gate formed on a second sidewall of the desired one of the first control gates, wherein the second sidewall spacer control gate further extends between the desired one of the first control gates and an opposite adjacent one of the first control gates.

34. The memory of claim 22, wherein the first and second sidewall spacer control gates include polysilicon.

35. The memory of claim 22, further comprising a silicide formed on the first and second sidewall spacer control gates.

36. The memory of claim 22, further comprising a silicide formed on the first control gate and on the first and second sidewall spacer control gates.

37. The memory of claim 22, wherein the charge storage regions are programmable via a process of hot carrier injection.

38. An integrated circuit having a non-volatile memory comprising:

a semiconductor substrate;

at least two buried bit lines formed within the semiconductor substrate, wherein the buried bit lines define boundaries that delineate the buried bit lines from an active region disposed between the buried bit lines;

a charge storage stack overlying the semiconductor substrate;

a first control gate overlying the charge storage stack;

an insulating liner overlying the first control gate; and

first and second sidewall spacer control gates formed adjacent to first and second sidewalls of the first control gate, respectively, the first and second sidewall spacer control gates being separated from the first control gate by at least the insulating liner, wherein multi-bit programmable charge storage regions are created within the charge storage layer beneath respective ones of the control gates.